

WHAT IS CLAIMED IS:

1 1. A TFT array substrate for use in a liquid crystal display
2 device, the TFT array substrate comprising:

3 a gate line arranged in a transverse direction over a substrate;

4 a metallic oxide layer surrounding the gate line;

5 a data line arranged in a longitudinal direction perpendicular to
6 the gate line over the substrate;

7 a thin film transistor formed near the crossing of the gate and data
8 lines, the thin film transistor comprising:

9 a gate electrode over the substrate, the gate electrode
10 being extended from the gate line and surrounded by the
11 metallic oxide;

12 a gate insulation layer on the metallic oxide surrounding
13 the gate electrode;

14 an active layer and an ohmic contact layer formed on the
15 gate insulation layer;

16 a source electrode formed on the ohmic contact layer
17 over the gate electrode and extended from the data line; and

18 a drain electrode formed on the ohmic contact layer over
19 the gate electrode and spaced apart from the source
20 electrode;

21 a protection layer formed over said thin film transistor, the
22 protection layer having a drain contact hole that exposes a portion of the
23 drain electrode; and

24 a pixel electrode formed in a pixel region that is defined by the gate
25 and data lines, the pixel electrode contacting the drain electrode through
26 the drain contact hole.

1 2. A TFT array substrate according to claim 1, wherein the
2 metallic oxide is one of tantalum oxide (TaO_x), chrome oxide (CrO_x),
3 titanium oxide (TiO_x) and tungsten oxide (WO_x).

1 3. A TFT array substrate according to claim 2, wherein the gate
2 line and the gate electrode are copper (Cu).

1 4. A TFT array substrate according to claim 1, further
2 comprising: a buffering layer between the substrate and the gate line
3 and gate electrode.

1 5. A TFT array substrate according to claim 4, wherein the

2 metallic oxide is one of tantalum oxide (TaO_x) and titanium oxide (TiO_x)
3 that are respectively made from tantalum (Ta) and titanium (Ti).

1 6. A TFT array substrate according to claim 4, wherein the
2 buffering layer is one of tantalum nitride (TaN) and titanium nitride
3 (TiN).

1 7. A TFT array substrate according to claim 4, wherein the
2 buffering layer is one of silicon nitride (SiN_x) and silicon oxide (SiO_2).

1 8. A method of forming a TFT array substrate for use in a
2 liquid crystal display device, comprising:

3 forming a first metal layer over a substrate;

4 forming a second metal layer on the first metal layer;

5 patterning the first and second metal layers so as to form a gate
6 line and a gate electrode;

7 thermally-treating the substrate having the patterned first and
8 second metal layers so as to diffuse material from the patterned first
9 metal layer over the patterned second metal layer and then to form a

10 metallic oxide layer surrounding the second metal layer by oxidizing the
11 diffused material of the first metal layer;

12 forming a gate insulation layer on the substrate, the gate line and
13 the metallic oxide layer;

14 forming an amorphous silicon layer on the gate insulation layer;

15 forming an impurity-doped amorphous silicon layer on the
16 amorphous silicon layer;

17 forming a third metal layer on the impurity-doped amorphous
18 silicon layer;

19 patterning the third metal layer so as to form a data line, a source
20 electrode and a drain electrode;

21 patterning the impurity-included amorphous silicon layer using
22 the patterned third metal layer as masks so as to form an ohmic contact
23 layer and a channel region in the amorphous silicon layer between the
24 source and drain electrodes;

25 forming a protection layer on the amorphous silicon layer and on
26 the patterned third metal layer;

27 patterning the protection layer, the amorphous silicon layer and
28 the gate insulation layer except portions that correspond to the
29 patterned third metal layer and channel region;

30 depositing a transparent conductive material in a pixel region that
31 is defined by the gate and data lines; and

32 patterning the transparent conductive material so as to form a
33 pixel electrode that contacts the drain electrode.

1 9. A method according to claim 8, wherein the first metal layer
2 is one of tantalum (Ta), chrome (Cr), titanium (Ti) and tungsten (W).

1 10. A method according to claim 9, wherein the metallic oxide
2 layer is one of tantalum oxide (TaO_x), chrome oxide (CrO_x), titanium
3 oxide (TiO_x) and tungsten oxide (WO_x).

1 11. A method according to claim 8, wherein the second metal
2 layer is copper (Cu).

1 12. A method according to claim 8, wherein the third metal layer
2 is one of chrome (Cr), tantalum (Ta), titanium (Ti), tungsten (W) and
3 molybdenum (Mo).

1 13. A method according to claim 8, further comprising: forming
2 a buffering layer on the substrate before forming the first metal layer.

1 14. A method according to claim 13, wherein thermal treatment
2 of the substrate is performed at a temperature of greater than 400°C.

1 15. A method according to claim 13, wherein the buffering layer
2 is one of tantalum nitride (TaN) and titanium nitride (TiN).

1 16. A method according to claim 13, wherein the buffering layer
2 is one of silicon nitride (SiN_x) and silicon oxide (SiO₂).

1 17. An insulated conductor structure for use in a TFT array
2 substrate of a liquid crystal display device, the conductor structure
3 comprising:

4 a substrate;

5 a metallic conductive line arranged over said substrate;

6 a metallic conductive electrode arranged over said substrate and
7 branching off said conductive line;

8 a metallic oxide layer surrounding said gate line; and
9 an insulation layer on said conductive line and said metallic oxide
10 layer.

1 18. The conductor structure according to claim 17, wherein said
2 metallic oxide is one of tantalum oxide (TaO_x), chrome oxide (CrO_x),
3 titanium oxide (TiO_x) and tungsten oxide (WO_x), respectively.

1 19. The conductor structure according to claim 18, further
2 comprising a buffering layer between the substrate and each of said
3 conductive line and said conductive electrode.

20. The conductor structure according to claim 19, wherein the buffering layer is one of tantalum nitride (TaN), titanium nitride (TiN), silicon nitride (SiN_x) and silicon oxide (SiO₂).

1 21. The conductor structure according to claim 17, wherein said
2 conductive line is a gate line and said conductive electrode is a gate
3 electrode.

1 22. The conductor structure of claim 17, wherein said
2 conductive line and said conductive electrode are made of copper (Cu).

1 23. A method of forming an insulated conductor structure for
2 use in a TFT array substrate of a liquid crystal display device, the
3 method comprising:

4 providing a substrate;

5 forming a first metal layer over a substrate;

6 forming a second metal layer on the first metal layer;

7 patterning the first and second metal layers so as to form a
8 conductive line and a conductive electrode thus defining an intermediate
9 structure;

10 thermally treating said intermediate structure so as to diffuse
11 material from the patterned first metal layer over the patterned second
12 metal layer and then to form a metallic oxide layer surrounding the
13 patterned second metal layer; and

14 forming an insulation layer on the substrate, the conductive line
15 and said metallic oxide layer.

1 24. The method according to claim 23, wherein the first metal
2 layer is one of tantalum (Ta), chrome (Cr), titanium (Ti) and tungsten (W)
3 and the metallic oxide is one of tantalum oxide (TaO_x), chrome oxide
4 (CrO_x), titanium oxide (TiO_x) and tungsten oxide (WO_x), respectively.

1 25. The method according to claim 23, wherein the second metal
2 layer is copper (Cu).

1 26. A method according to claim 23, further comprising:
2 forming a buffering layer on the substrate before forming the first
3 metal layer.

1 27. A method according to claim 26, wherein the buffering layer
2 is one of tantalum nitride (TaN), titanium nitride (TiN), silicon nitride
3 (SiN_x) and silicon oxide (SiO₂).